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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,755	11/19/2003	Stephen H. Tang	80107.038US1	6175

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EXAMINER

MAI, SON LUU

ART UNIT	PAPER NUMBER
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2827

DATE MAILED: 05/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/716,755

Applicant(s)

TANG ET AL.

Examiner

Son L. Mai

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 19 November 2003 and 08 March 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-30 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-30 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 March 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 3-08-04.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement submitted on 03-08-04 has been considered by the examiner.

Drawings

2. The drawings were received on 03-05-04. These drawings are acceptable.

Specification

3. The disclosure is objected to because the descriptions on pages 10 and 11 are not consistent. On page 10, the transistor 408 is a selected transistor and on page 11, the selected transistor is transistor 406. According to figure 5, the selected transistor should be the transistor 408. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-30 are rejected under 35 U.S.C. 102(e) as being anticipated by Fazan et al. (U.S. Patent Application Publication US 2004/0021137 A1) (hereinafter "Fazan").

Regarding claim 1, Fazan teaches a method of writing data to a row (track 40 in figure 13) of single transistor memory cells (cells 32) wherein an applied gate voltage

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when writing a "0" is different than an applied gate voltage when writing a "1" (see paragraphs [0098] and [0099], an applied gate voltage is brought to -1.5V and to $+1\text{V}$).

Regarding claim 2, Fazan teaches that writing data comprises writing data to single transistor floating-body memory cells (cells 32 in figure 1).

Regarding claim 3, Fazan teaches that applying drain voltages to either charge or discharge bodies of the single transistor memory cells (paragraphs [0098] and [0099]).

Regarding claim 4, Fazan teaches that applying a drain voltage to charge bodies comprises creating impact ionization currents (paragraph [0077]).

Regarding claim 5, Fazan teaches at paragraph [0088] applying a drain voltage to discharge bodies comprises creating a voltage differential to turn on a diode.

Regarding claim 6, Fazan teaches that the applied gate voltage when writing a "0" is less than the applied gate voltage when writing a "1" (paragraphs [0098] and [0099] explain writing a "0" and a "1" with the applied gate voltage of $+1\text{V}$ and -1.5V . Here, writing "0" is represented by a charged body with the applied gate voltage -1.5V .

Regarding claim 7, Fazan teaches a method comprising writing data to floating-body memory cells in two phases (write "0" and write "1"; see paragraphs [0098] and [0099]), wherein each of the two phases utilizes a different word line voltage on a word line ($+1\text{V}$ and -1.5V ; see paragraphs [0098] and [0099]).

Regarding claim 8, Fazan teaches that a first phase writes to a first subset of memory cells coupled to the word line (writing to one cell which is coupled to track 40₂ in figure 13).

Regarding claim 9, Fazan teaches that the first phase discharges (writing "0") floating bodies of the first subset of memory cells.

Regarding claim 10, Fazan also teaches that the first phase comprises reducing a voltage on at least one bit line to turn on a diode formed at least partially by a floating body of a transistor (embodiment in figure 8 shows a forward-biased diode when the bit line is brought to $-2V$.)

Regarding claim 11, Fazan shows in figure 13, a second phrase (writing "1") writes to a second subset (other cells coupled to track 40₂) of memory cells coupled to the word line.

Regarding claim 12, Fazan teaches that the second phase (writing "1") charges floating bodies of the second subset of memory cells.

Regarding claim 13, Fazan teaches that the first phase (writing "0") includes providing a first drain voltage ($-2V$) on the first subset of memory cells and a second drain voltage ($0V$) on cells other than the first subset; and the second phase (writing "1") includes providing a third drain voltage ($-2V$) on the second subset of memory cells and a fourth drain voltage ($0V$) on cells other than the second subset.

Regarding claim 14, Fazan teaches a method (paragraphs [0098] and [0099]) comprising: providing a first voltage ($-1.5V$) on a word line (track 40₂) coupled to a plurality of memory cells; writing "0" to at least one of the plurality of memory cells; providing a second voltage ($+1V$) on the word line; and writing "1" to at least one of the plurality of memory cells.

Regarding claim 15, Fazan shows in figure 13, each of the plurality of memory cells includes a single transistor (transistor 32).

Regarding claim 16, Fazan shows in figure 13, the word line (track 40₂) is coupled to gates of the single transistors (transistors 32).

Regarding claim 17, Fazan teaches that the second voltage (+1V) is higher than the first voltage (-1.5V).

Regarding claim 18, Fazan shows in figure 1, each of the plurality of memory cells (transistor 32) comprising a floating-body transistor.

Regarding claim 19, Fazan teaches that writing a "0" comprises providing a voltage on a bit line to turn on a diode (embodiment in figure 8 shows a forward-biased diode when the bit line is brought to -2V.)

Regarding claim 20, Fazan teaches at paragraph [0077] that writing a "1" comprises providing a voltage on a bit line to generate an impact ionization current.

Regarding claim 21, Fazan teaches an apparatus (figure 13) comprising: a row of memory cells (coupled to track 40), and a word line driver (46) coupled to the row of memory cells, the word line driver to generate a first voltage (-1.5V) when writing a "0" and a second voltage (+1V) when writing a "1".

Regarding claims 22 and 23, Fazan teaches that the word line driver (46) is adapted to generate at least four different voltages (0V, 0.8V, +1V, and -1.5V; see figures 2-7d).

Regarding claim 24, Fazan teaches that the row of memory cells comprise floating-body transistors (figure 1).

Regarding claim 25-30, all the claimed features have been discussed in the preceding paragraphs. The antenna, and the first and second integrated circuits of claim 28 recite only intended used of the memory device as set forth in the preceding claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Besides the U.S. Patent Application Publication US 2004/0021137 A1, other references in form PTO-892 disclose floating-body single transistor memory cells.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Son L. Mai whose telephone number is 571-272-1786. The examiner can normally be reached on 8am to 6pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoai Ho can be reached on 571-272-1777. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



**SON L. MAI
PRIMARY EXAMINER**